EPFL

VLSC

Manticore

Hardware-Accelerated RTL Simulation with Static Bulk-Synchronous Parallelism

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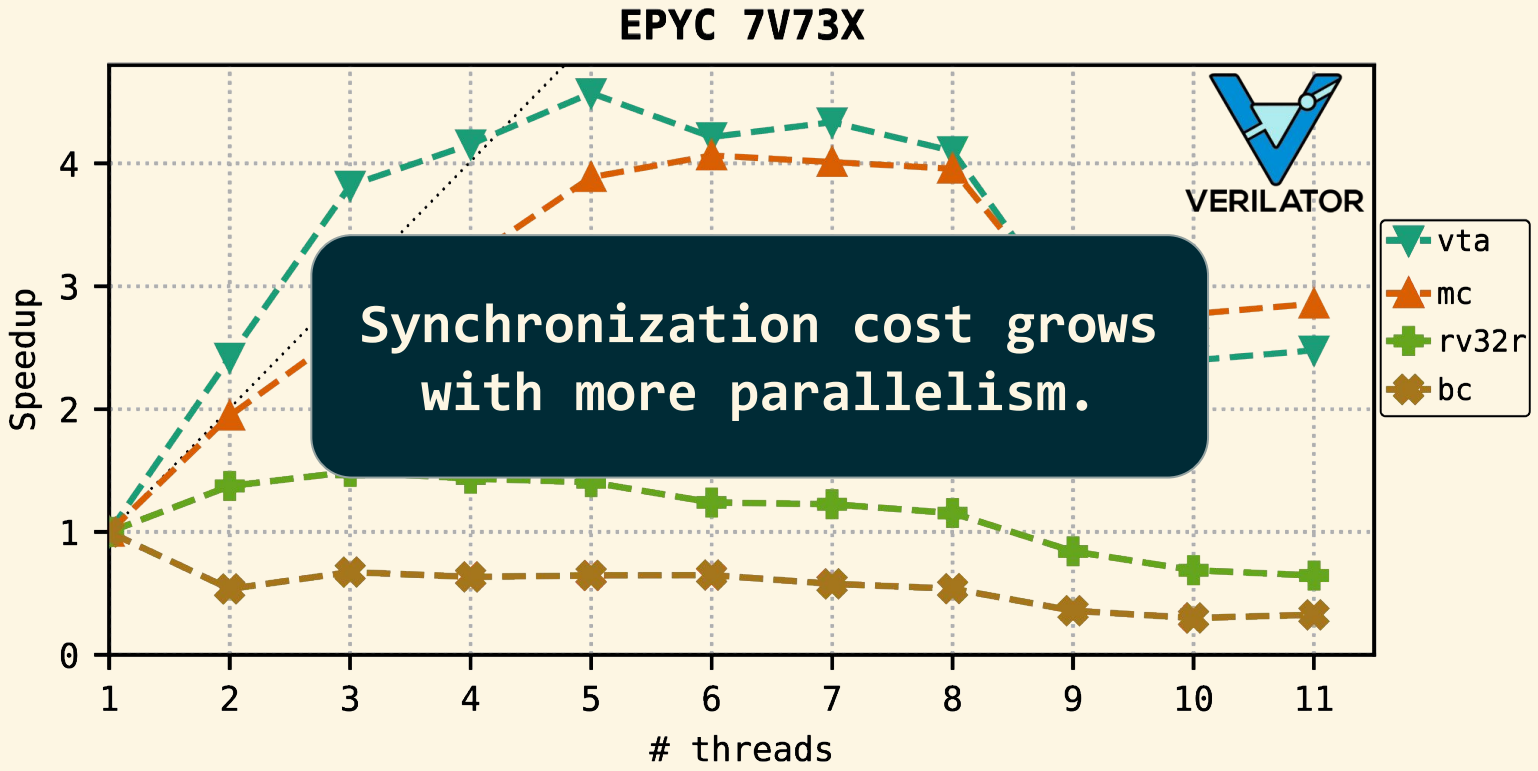
Parallel RTL Simulation is Hard!



Key Idea:

Reduce sync. overhead through **static scheduling**!

How?

Build a machine, **Manticore**, that can be statically scheduled!

Manticore: A Statically Scheduled Manycore

- RTL simulation accelerator
  - 225 message-passing cores
- Chip-wide lockstep execution
  - *“Compile-time” sync.*